



H61H2-D

Rev : A

ECS CONFIDENTIAL

TABLE OF CONTENTS

Page	Index
1	Cover Page
2	Block Diagram
3	CPU - DMI/FDI/PEG
4	CPU - MISC
5	CPU - DDR3
6	CPU - PWR/GND
7	DDR3 - CH_A_DIMM1
8	DDR3 - CH_B_DIMM3
9	VCore & VAXG-RT8859A
10	VCore & VAXG- RT9616
11	RT8121 DC/DC CPUVTT
12	DC/DC VDIMM/DDR_VTT/5VDUAL
13	Front Panel,FAN,PowerConn
14	PCH - DMI/PCIe/PE/USB
15	PCH - SATA / CLK
16	PCH - MISC, Strap Function
17	PCH - DP/VGA/FDI
18	PCH - PWR
19	PCH - GND
20	Slot - PCI-EX16/PCI-EX1
21	DVI&HDMI CONN&COM&PSUSB
22	USB/SATA/SPI
23	SIO-IT8758BX
24	AUDIO ALC892/ALC662(CHIP)
25	AUDIO ALC892/ALC662(PANEL)

REVISION HISTORY:

Page	Index	Rev	Date	Notes
26	GND,104	V.A	2010/11/09	Change from H67H2-M3: 1. Del PCI SLOT *2&Add PCIe1 slot *2 2. Del PCI Bridge IT8893CX 3. Add TPM/LPT/LPC DEBUG HEADER 4. Super IO change to IT8728CX 5. Chipset change to H61
27	PCIE LAN RTL8111E/8105E,USBLAN CONN			
28	USB3.0 NEC 720200,USB3.0 CONN			
29	Power Delivery	V.1.0	2010/12/06	Change from H61H2-M5:VA 1.P23 change 5V_CTRL FOR EZ_CHANGE 2.P24 CHANGE Cg FOR COLAY VIA 1705CE 2010/12/06 FQ 3.P23 ADD VIN2 VIN5 VIN6 20101208 ADD FOR RESERVE 2010/12/09 4.P25 change front line damping resistor 75ohm to 16ohm when in stall VIA codec 5. P13 Add 4PIN SYSFAN2 1211 FQ Change 12V EC, MC110/MC111 10U-16VY-12 6. P22 Change SATA1/2 footprint 90 7. P23 PCH_THRM_L NO connect ,PULL HIGH VCC3 8. P28 USB3 USE NEC720200 9. P9/P10 PWM RT8859MGQW + RT9612BGS SUS RT8859AGQW + RT9619APS 10.P21/22 Change USBX4 TO USBX2 PS2 Change TO PSUSB 1213 11.P13 CHANGE 4PIN SYS&PWR FAN TO 3PIN FAN
30	Power Sequence, Reset Diagram			
31	Clock Distribution	V.A	2011/02/10	Change from H61H2-M5:V1.0 1.P22 Add F_USB3,USBPWR3(the same to USBPWR1) for F_USB3 Del USBX4,one UP7536AMA8S Change USBVCC3 the same to USBVCC2, Cut the U32(ESD for USB) and CMF10 Change SATA1/2(90D) to SATA1,SATA2(180D) 2.P27 Del USB3LAN Connector Add USB2LAN Paste the U32(ESD for USB) and CMF10 from P22 3.P23 Change SIO IT8728CX-->IT8758BX 4.P13 Del PWR_FAN 5.P12 Change ER97 to 196ohm for raise 3VSB Del IC raise voltage circuit 6.P17 Change VGA over DVI,change the VGA VALUE and Footprint 8.P15 Del CK_P33M_LPC with TPM and Del PCIe1x slot B,C Data and CLK 9.P26 Del TPM and LPT 10.P16 Del LPCPD_L with TPM 11.P20 Del two PCIe1x slot B,C and 6 Decoupling Cap for Del two PCIe1X 12.P24 Refer to Modular circuit ,change AUDIO to ALC892(colay ALC662) 13.P28 Add USB3.0X2 Connector(including ESD) 14.P4 Power Down Sequence Del VR_READY and CPUPWR_OK 15.P02 Update Block Diagram

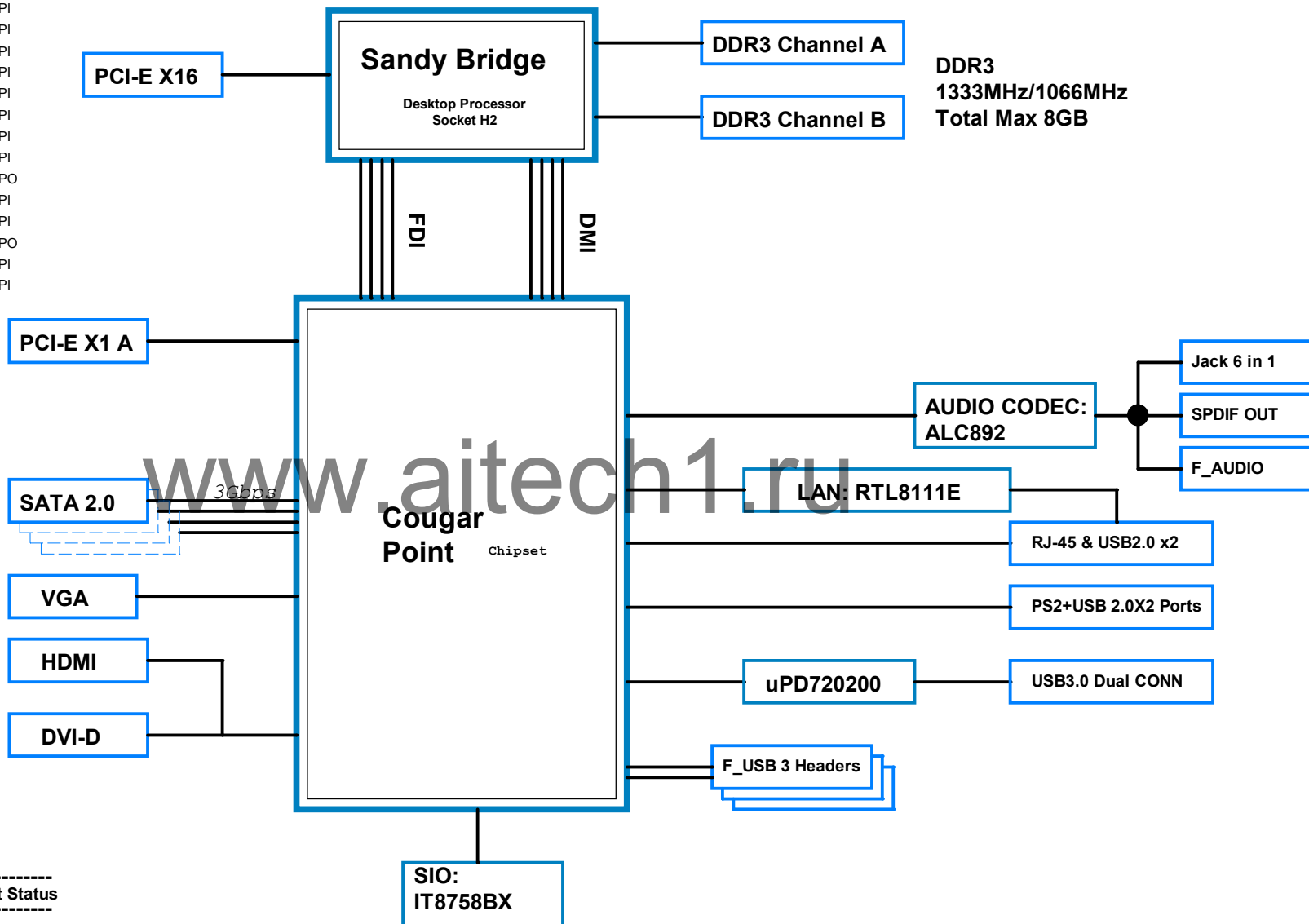
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NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

Elitegroup Computer Systems		
Title		
Cover Page		
Size	Document Number	Rev
Custom	H61H2-D	V:A
Date:	Tuesday, March 01, 2011	Sheet 1 of 31

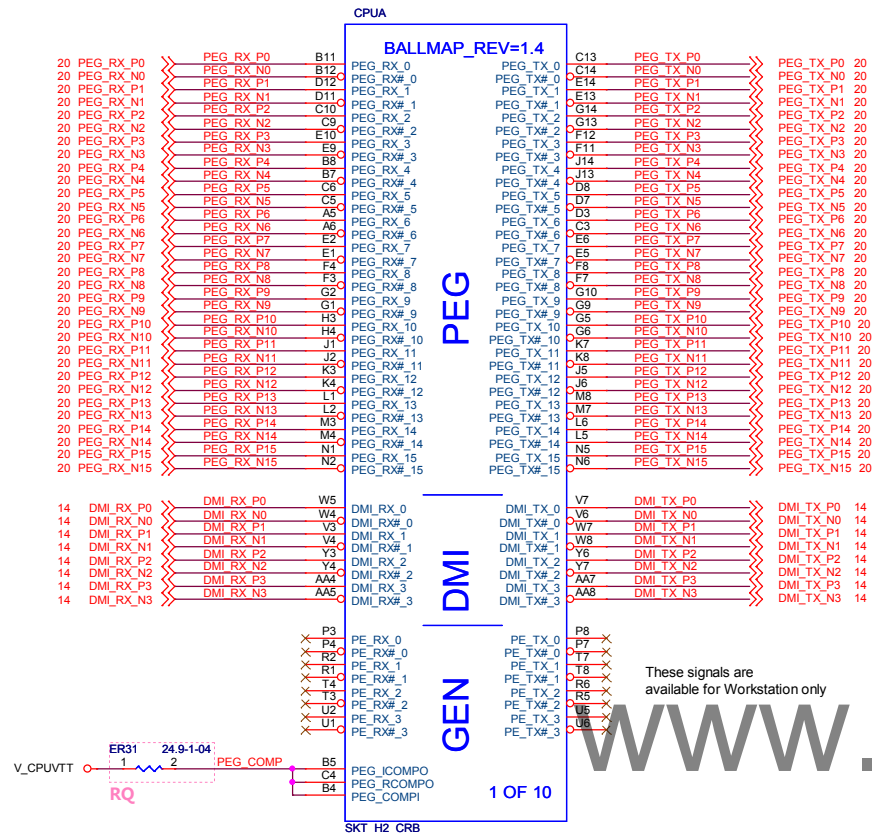
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

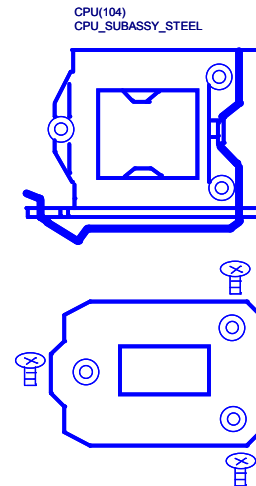


SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.



11-018-115021 CPU SMD SOCKET
SOCKET.CPU_LGA 1155P SMD.BLACK.PE115527-4041-01F.
LEAD-FREE.FOXCONN

20-800-004711 CPU SOCKET STEEL
SUBASSY.STEEL.LGA 1155P.W/
BACK PLATE.PT44A11-6401.LEAD-FREE(RoHS).FOXCONN

01D201-000060 PCH ES0

CPU - DMI/FDI/PEG	
Title	Document Number
Size	H61H2-D
Custom	Rev
Date: Tuesday, March 01, 2011	Sheet 3 of 31

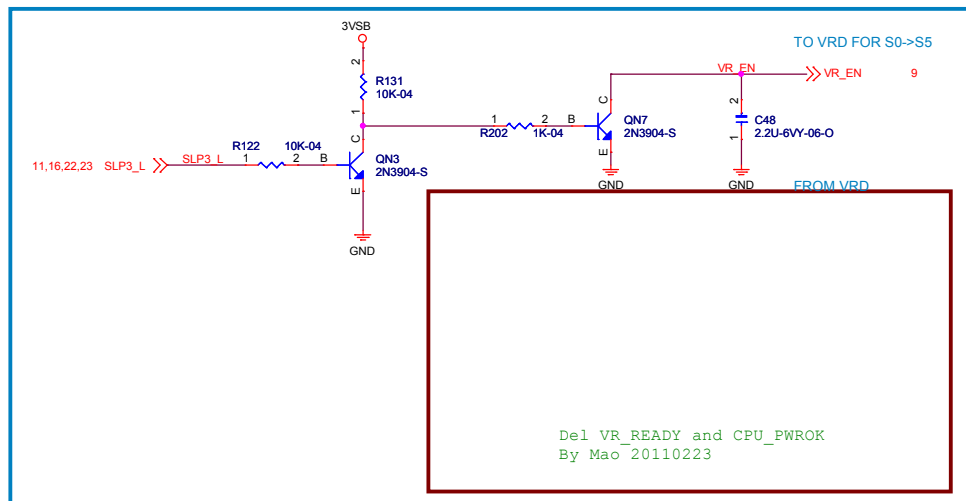
CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PECFGSEL[0]
6	*	*	PECFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X16	1	1
2 X8	0	1

CFG[5:6]:
 11=DEFAULT X16,
 01=X8,
 10=RESERVED,
 00=X8,X4,X4

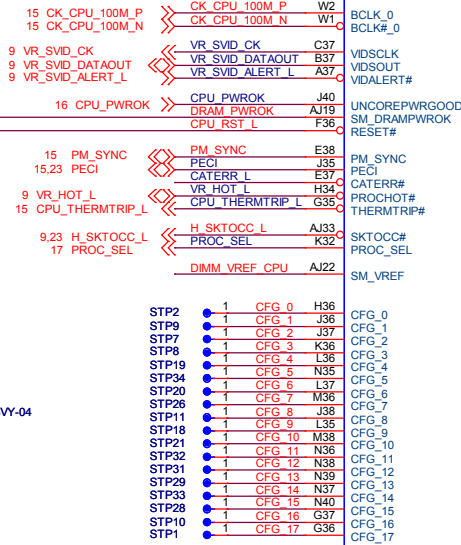
Power Down Sequencing Circuit



change test point for internal PU Jack05/25

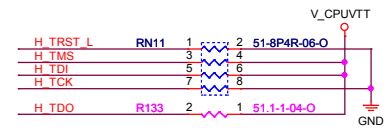
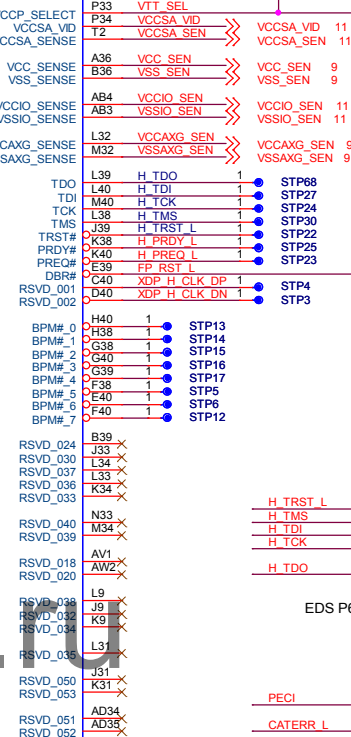
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BALLMAP_REV=1.4

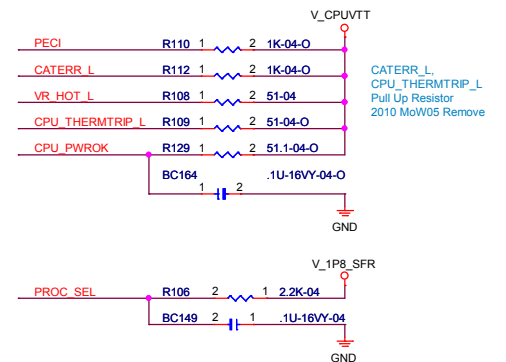


5 OF 10

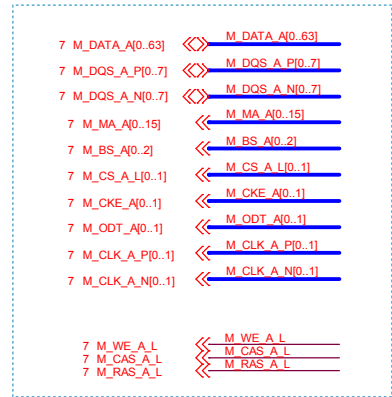
SKT_H2_CRB



EDS P68/132 has internal PU Jack05/25

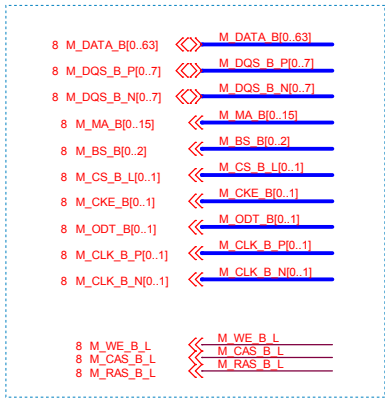


DMI/FDI termination voltage:
 DC coupled: TX/RX to VCC ISF sampled high
 DC coupled: TX/RX TO VSS IF sampled low
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap

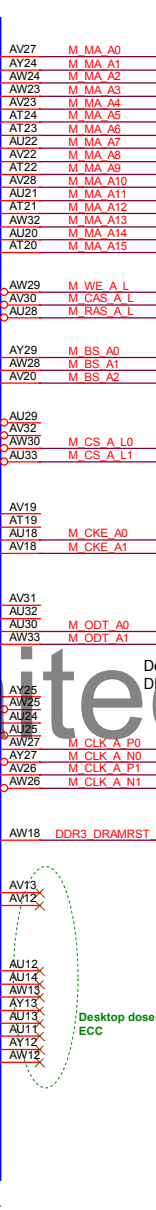
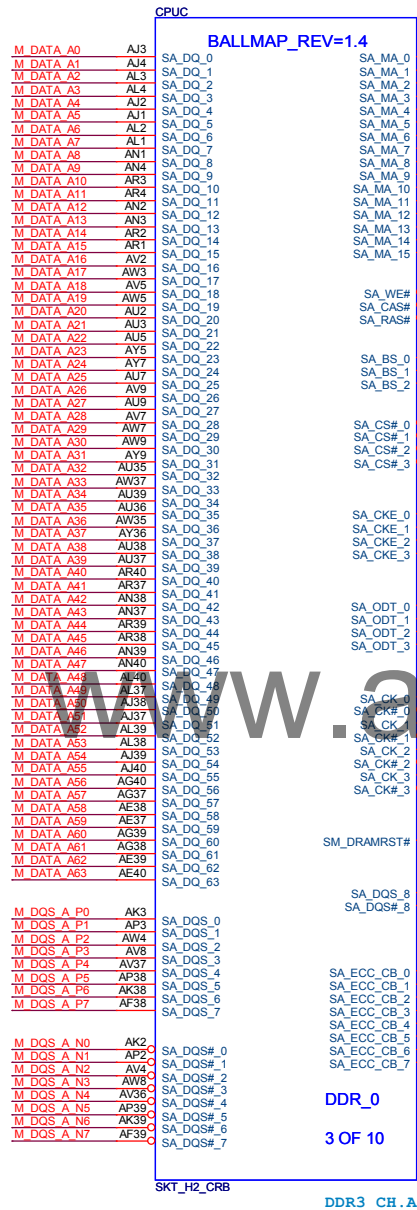


DDR3 CH.A

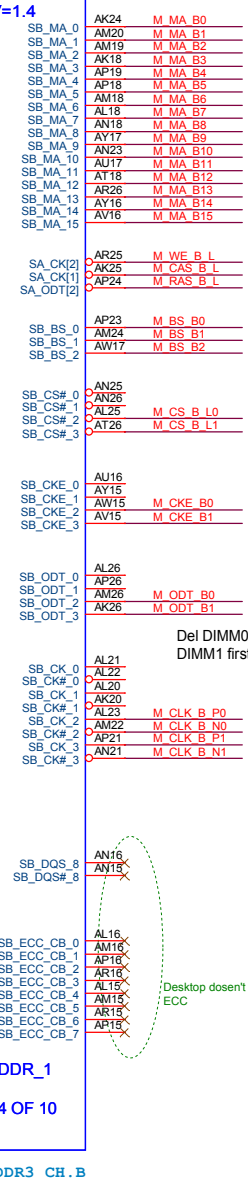
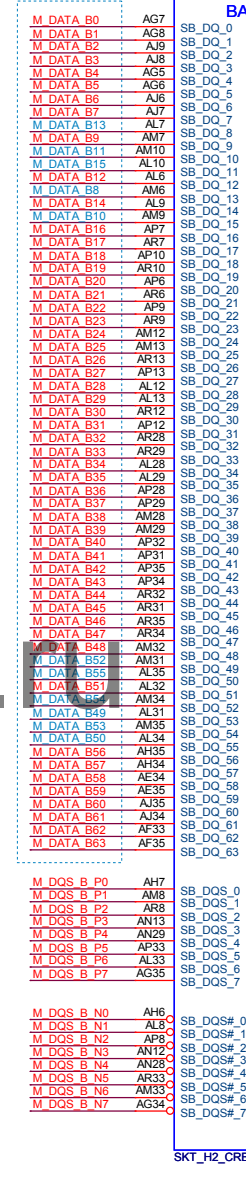
7,8 DDR3_DRAMRST_L << DDR3_DRAMRST_L

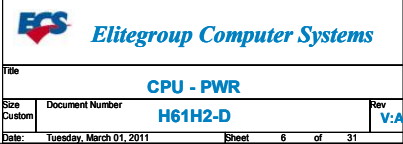


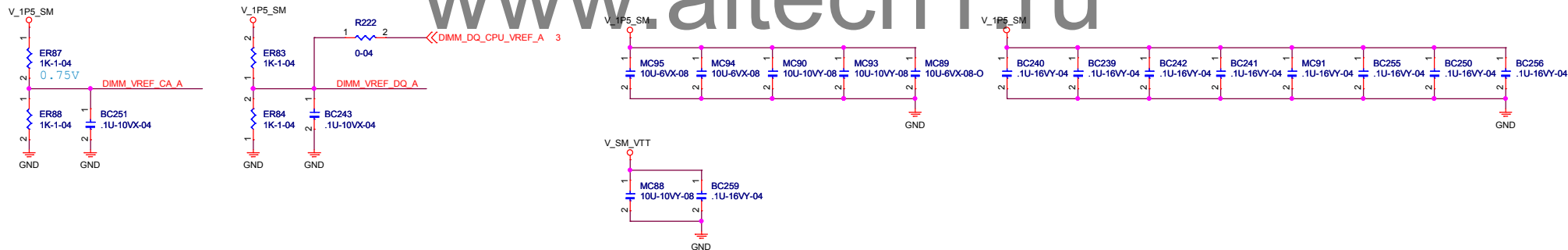
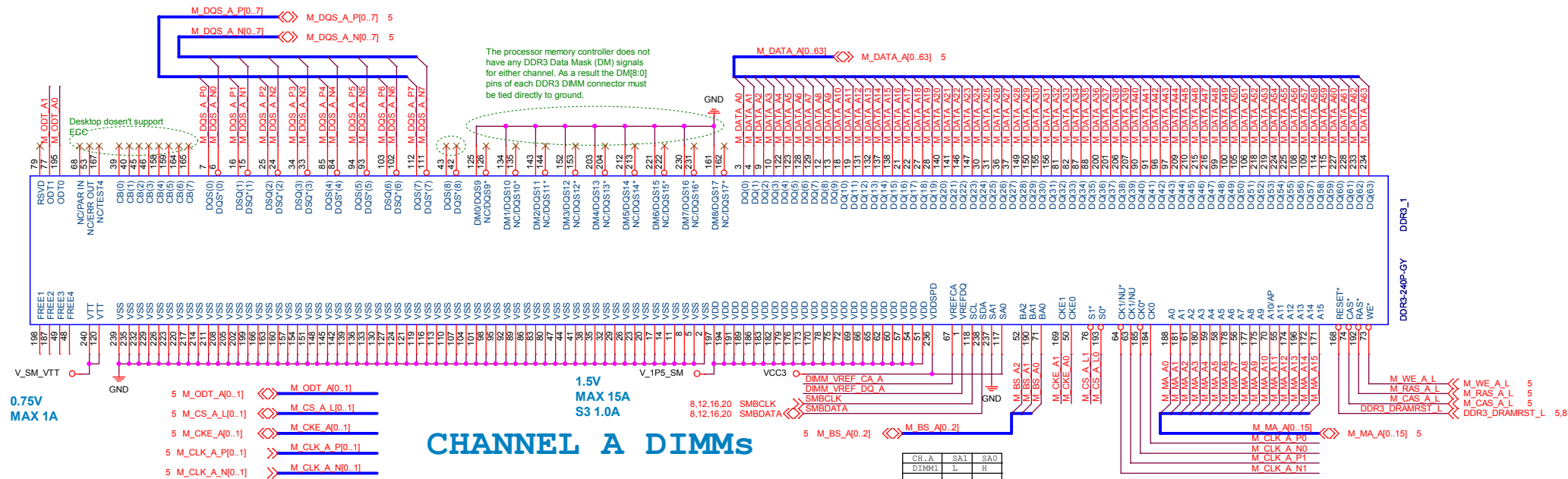
DDR3 CH.B



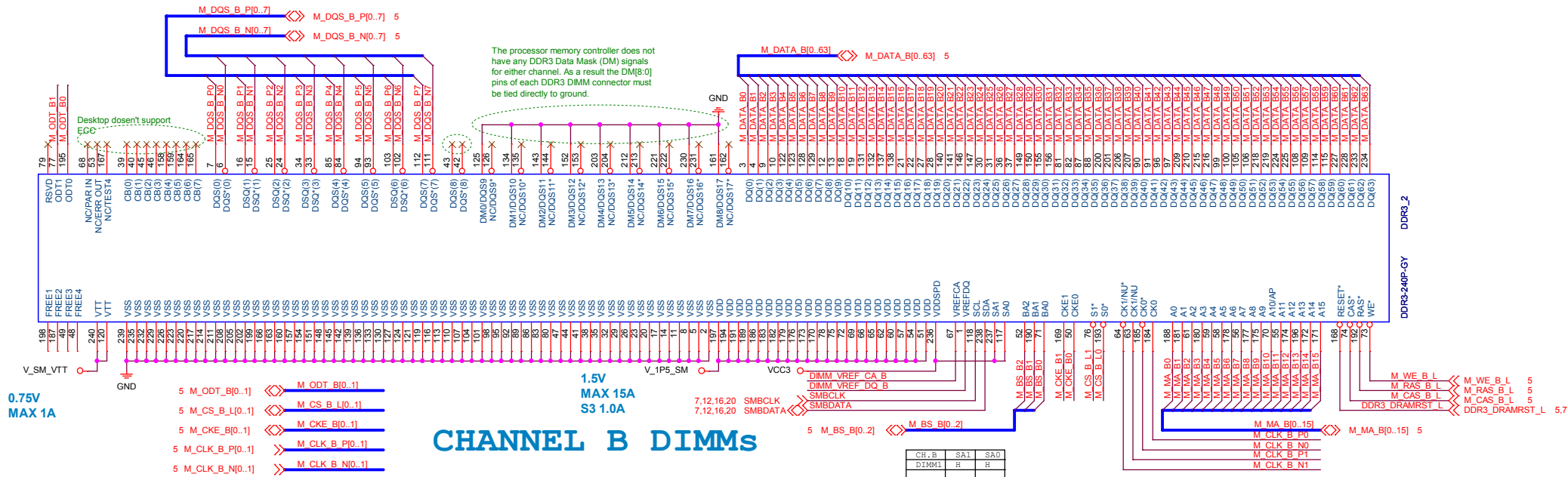
Pay Attention to This Part!







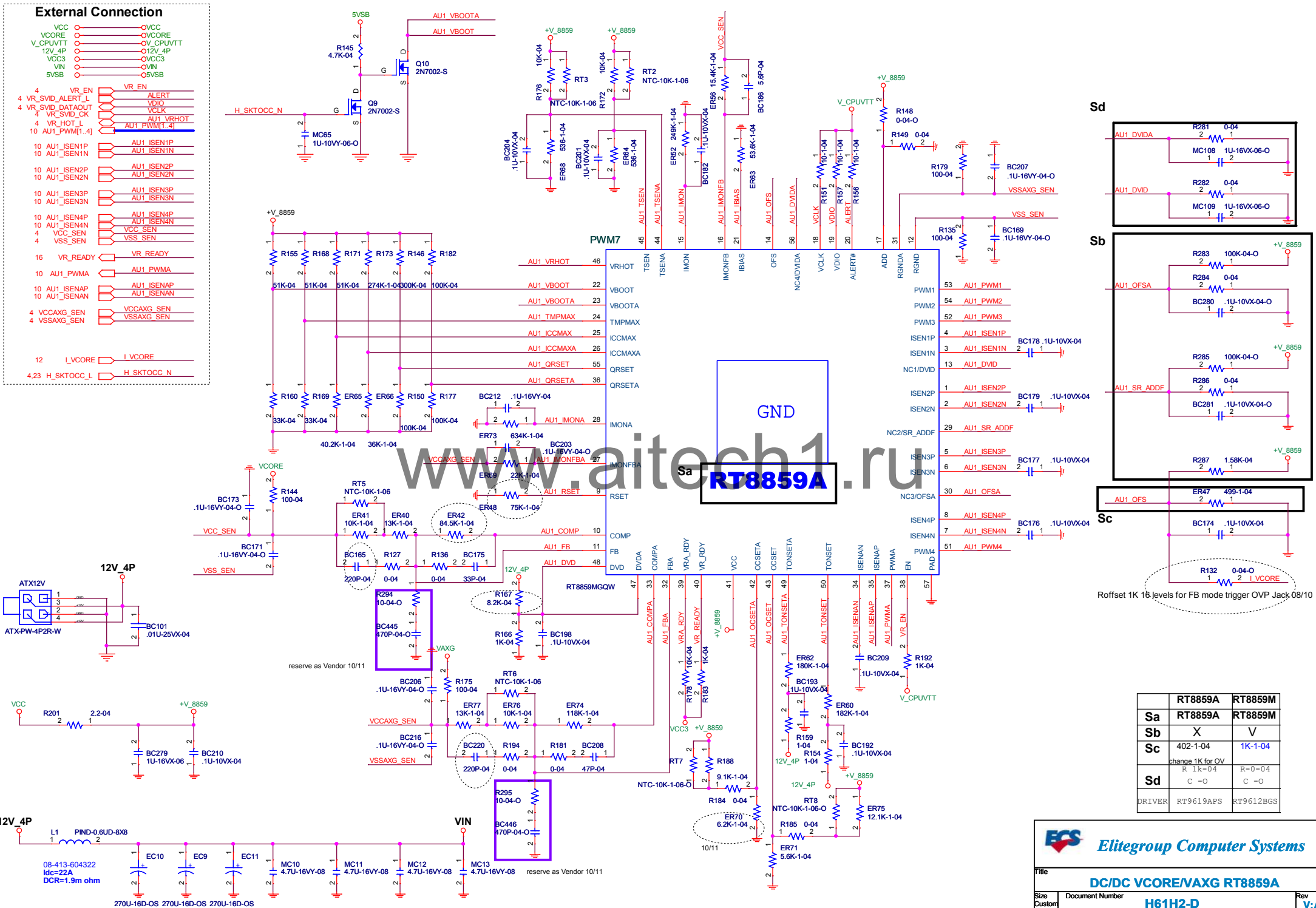
Del DIMM1 for always populate DIMM2 first Jack 05/13



Del DIMM3 for always populate DIMM4 first Jack 05/13

External Connection

Pin	Function	External Component
VCC		+VCC
VCORE		+VCORE
V_CPUVTT		+V_CPUVTT
12V_4P		+12V_4P
VCC3		+VCC3
V_M		+V_M
5VSB		+5VSB
4 VR_EN		+VR_ALERT
VR_SVD_ALERT_L		+VDDIO
4 VR_SVD_DATAOUT		+VCLK
4 VR_SVD_CK		+AU1_VRHOT
4 VR_HOT_L		+AU1_PWM[1..4]
10 AU1_PWM[1..4]		AU1_ISEN1P
10 AU1_ISEN1P		AU1_ISEN1N
10 AU1_ISEN2P		AU1_ISEN2N
10 AU1_ISEN2N		AU1_ISEN3P
10 AU1_ISEN3P		AU1_ISEN3N
10 AU1_ISEN4P		AU1_ISEN4N
10 AU1_ISEN4N		+VCC_SEN
4 VCC_SEN		+VSS_SEN
VSS_SEN		+VR_READY
16 VR_READY		AU1_PWMA
10 AU1_PWMA		AU1_ISENAP
10 AU1_ISENAP		AU1_ISENAN
10 AU1_ISENAN		+VCCXAG_SEN
4 VCCXAG_SEN		+VSSXAG_SEN
4 VSSXAG_SEN		I_VCORE
12 I_VCORE		H_SKT0OCC_N
4.23 H_SKT0OCC_L		



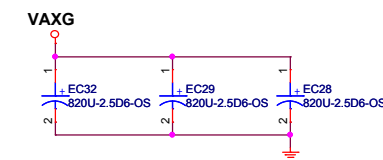
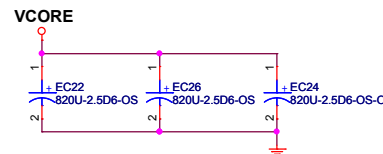
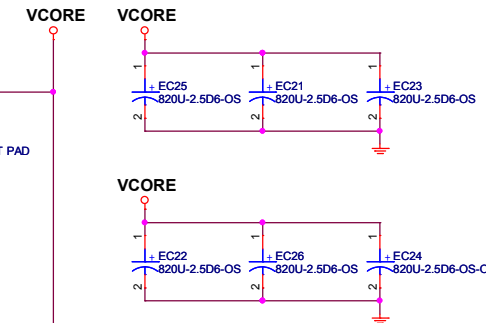
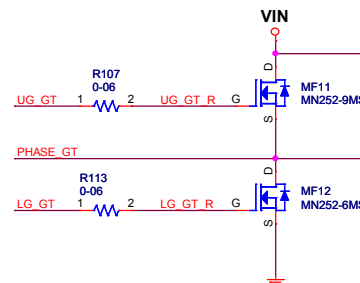
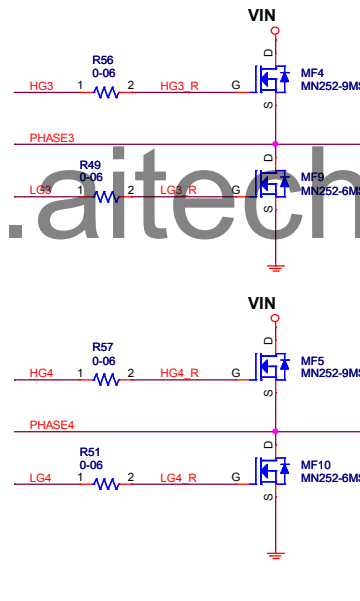
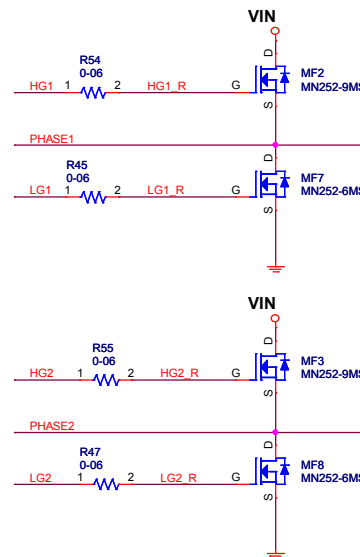
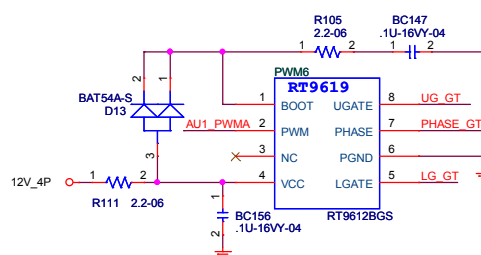
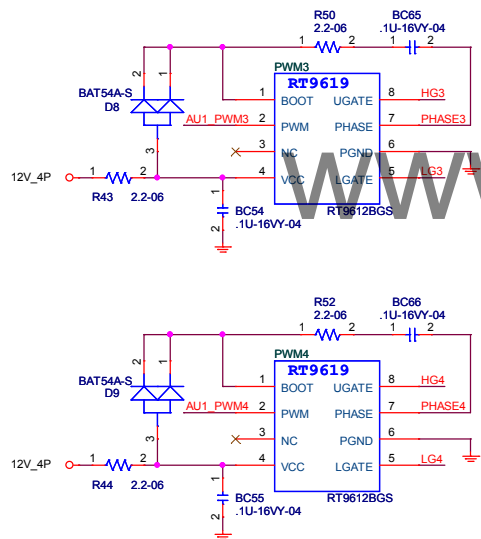
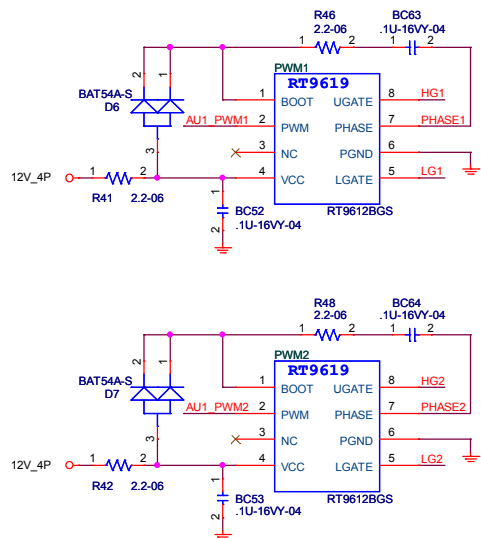
	RT8859A	RT8859M
Sa	RT8859A	RT8859M
Sb	X	V
Sc	402-1-04 change 1K for OV	1K-1-04
Sd	R 1k-04 C -O	R-0-04 C -O
DRIVER	RT9619APS	RT9612BGS

External Connection

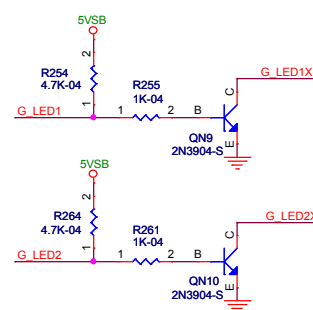
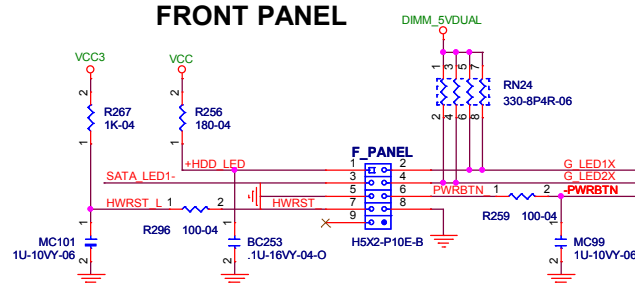
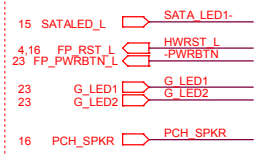
VCC ○ VCC
VCORE ○ VCCORE
12V_4P ○ 12V_4P
VCC3 ○ VCC3
VIN ○ VIN

9 AU1_PWM[1..4] AU1_PWM[1..4]
9 AU1_ISEN1P AU1_ISEN1P
9 AU1_ISEN1N AU1_ISEN1N
9 AU1_ISEN2P AU1_ISEN2P
9 AU1_ISEN2N AU1_ISEN2N
9 AU1_ISEN3P AU1_ISEN3P
9 AU1_ISEN3N AU1_ISEN3N
9 AU1_ISEN4P AU1_ISEN4P
9 AU1_ISEN4N AU1_ISEN4N
4,9 VCC_SEN VCC_SEN
4,9 VSS_SEN VSS_SEN

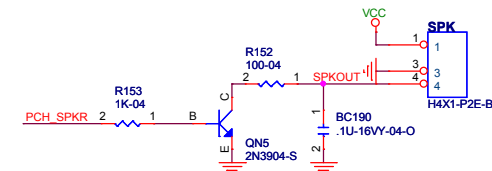
9 AU1_PWMA AU1_PWMA
9 AU1_ISENAP AU1_ISENAP
9 AU1_ISENAN AU1_ISENAN
4,9 VCCAXG_SEN VCCAXG_SEN
4,9 VSSAXG_SEN VSSAXG_SEN



External Connection



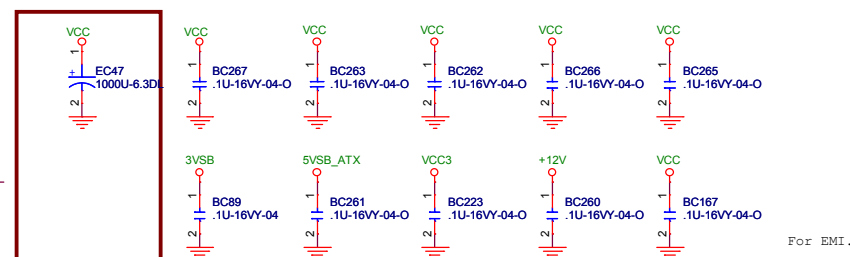
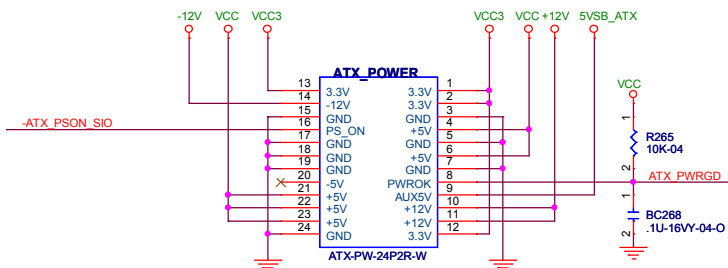
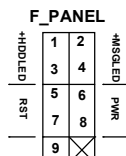
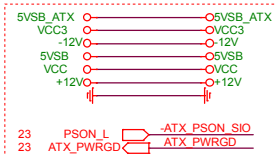
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	GB	YB	OFF	OFF



Add Electrolytic capacitor
 By Mao 20110223

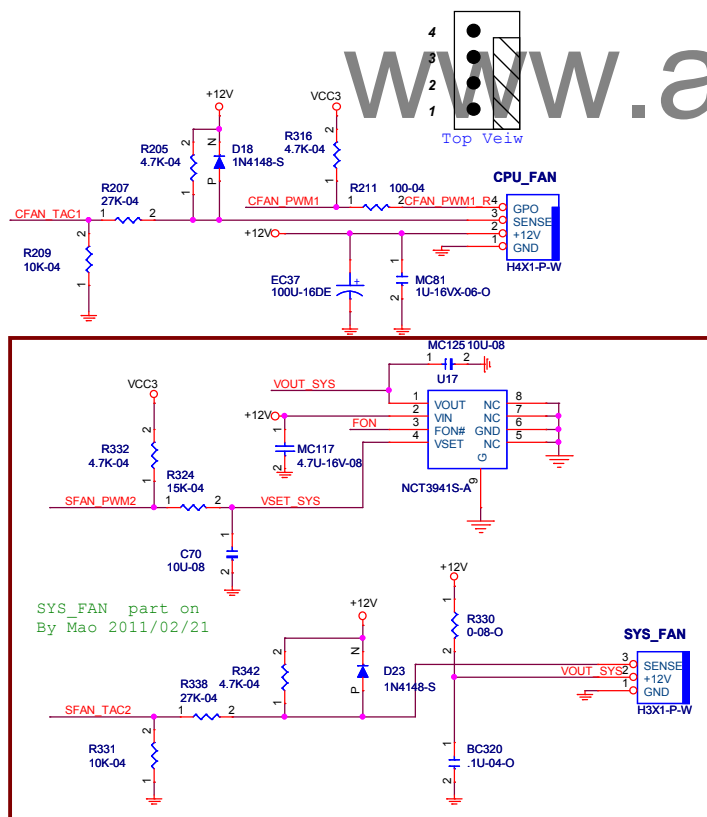
POWER CONNECTOR

External Connection



FAN

External Connection

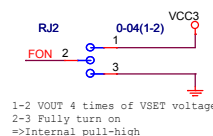


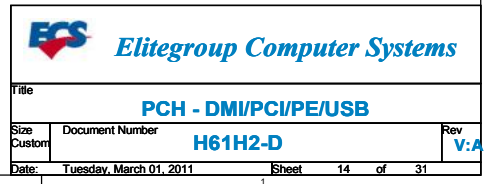
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Del 3 pin PWR_FAN (smart FAN)
 By Mao 2011/02/15

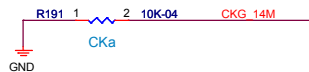
FQ 1217

Add 3 pin control Fan

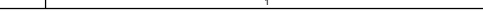


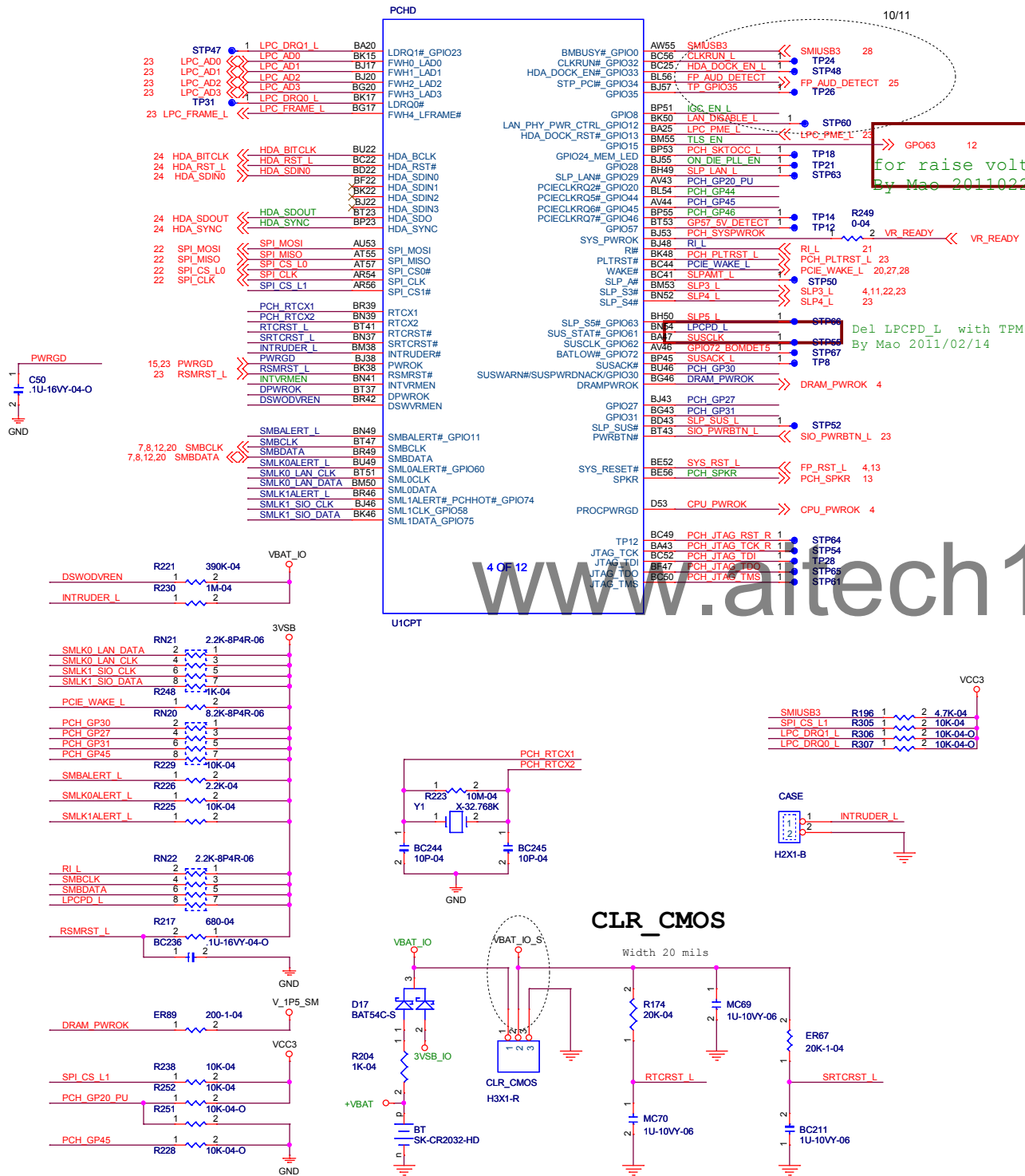


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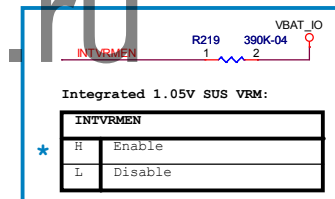
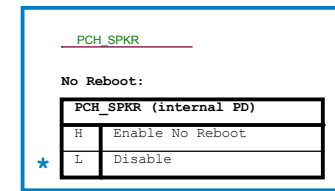
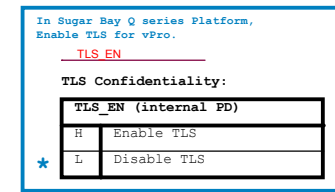
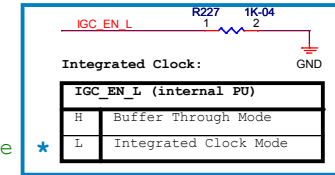


Stuff for Integrated Clock Mode

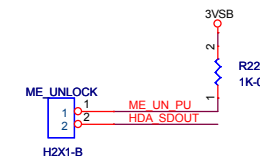
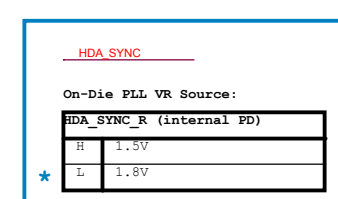
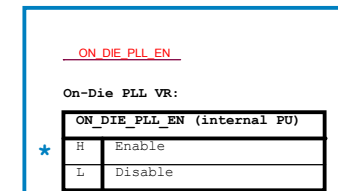
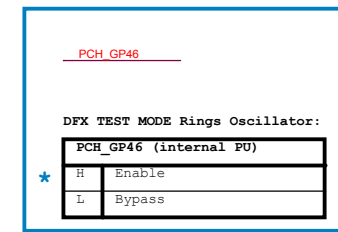
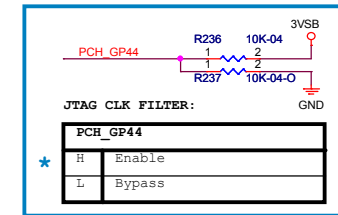
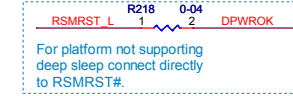




Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap. Default: Integrated Clock Mode. Doc. Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1

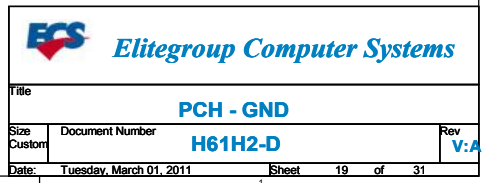


When Deep Sleep not implemented:
1. PCH_GP30, PCH_GP27 need to be Pull Up.
2. VCCDSV3_3 should be connected to +3VSB.
3. SLP_SUS_L, SUSACK_L left unconnected.
4. SUSWARN_L may be used as GPIO30 (Reference to 1.)

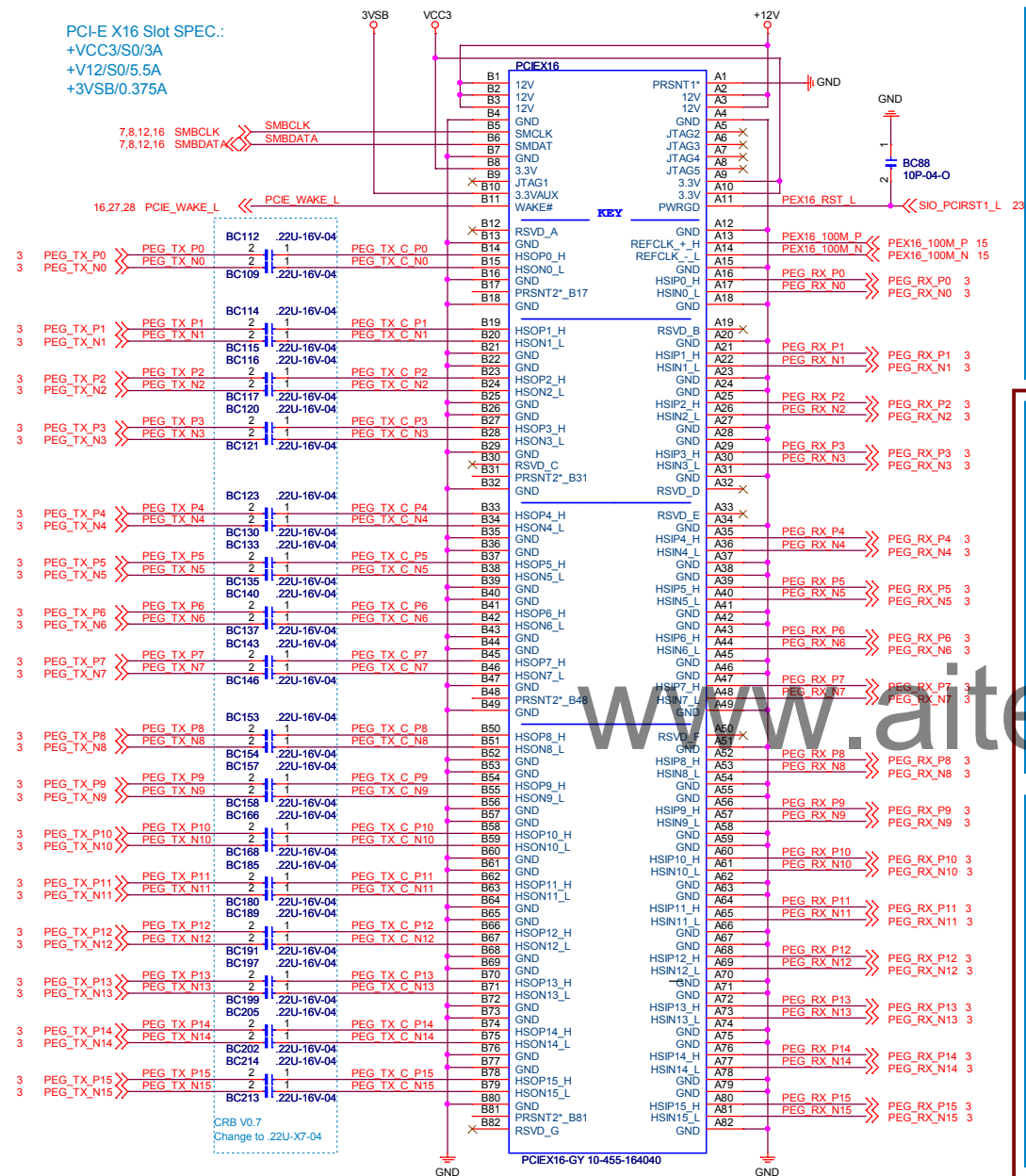


ME Enable/Disable

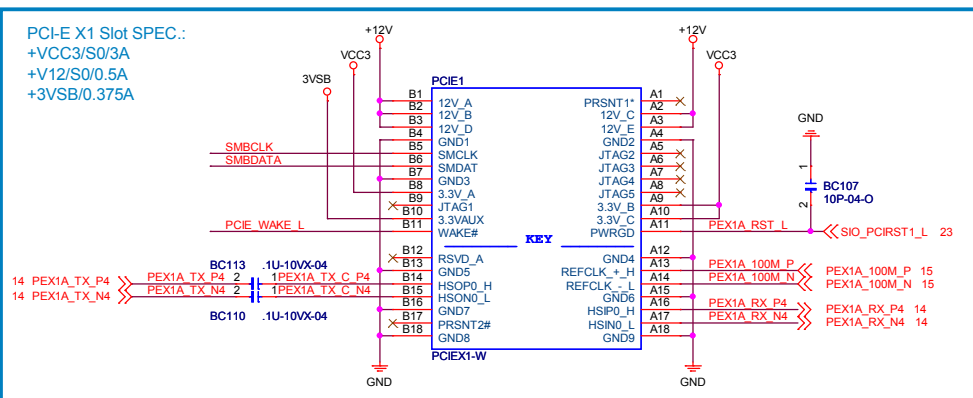
	ME_UNLOCK
1-2	UNLOCK
Float	LOCK



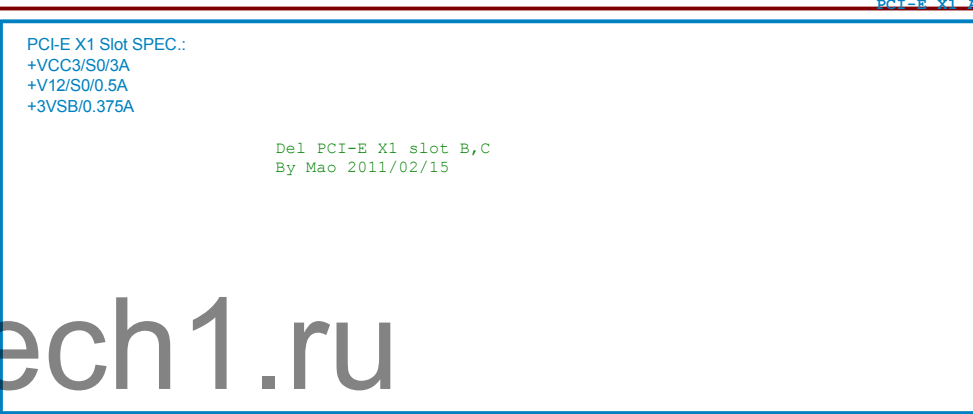
PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



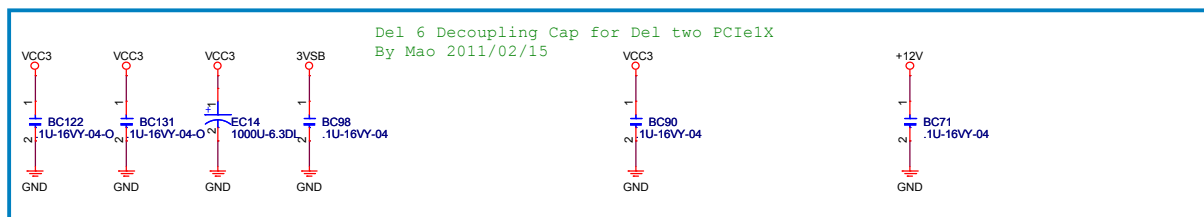
PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



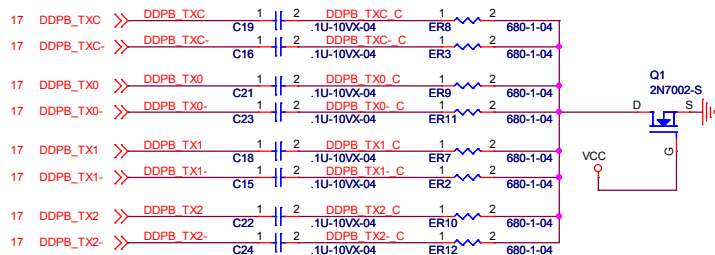
Del 6 Decoupling Cap for Del two PCIe1X
By Mao 2011/02/15



PCI-E X1 A Decoupling Cap.

ADD PCIe1 *2 1109 FQ

Title Slot - PCI-EX16/PCI-EX1	
Size Custom	Document Number H61H2-D
Date: Tuesday, March 01, 2011	Rev V: A
Sheet 20	of 31

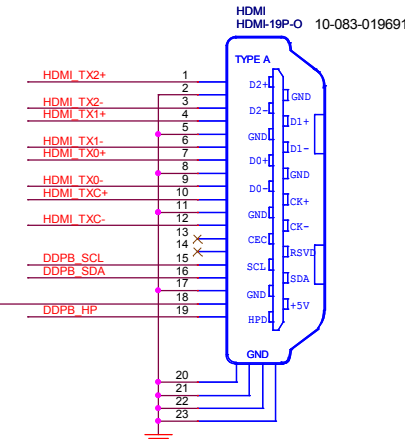
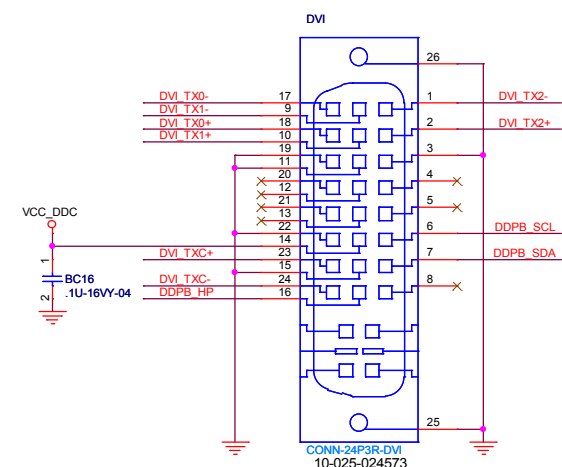
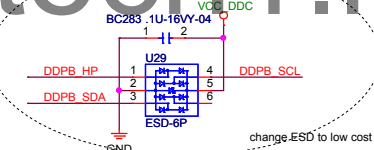
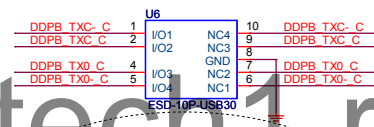
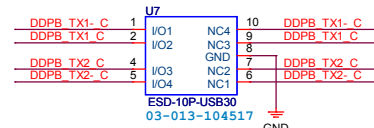
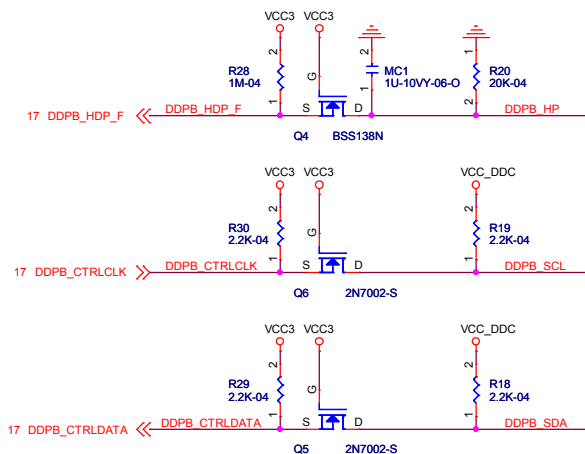
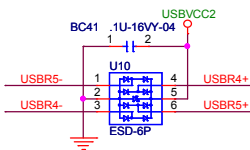
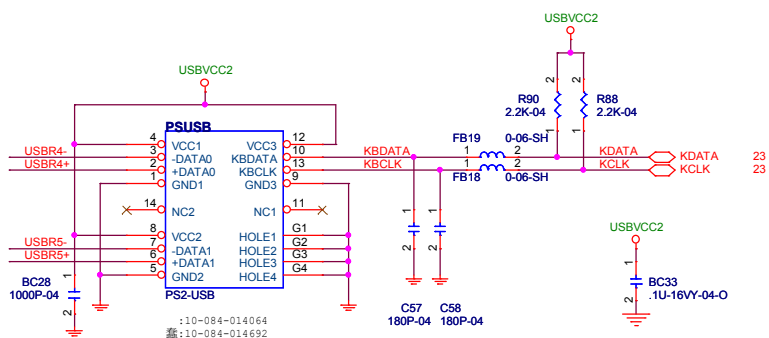
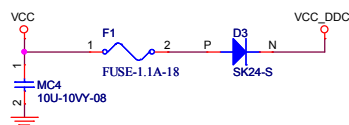


change DVI or HDMI must change GPIO in page15

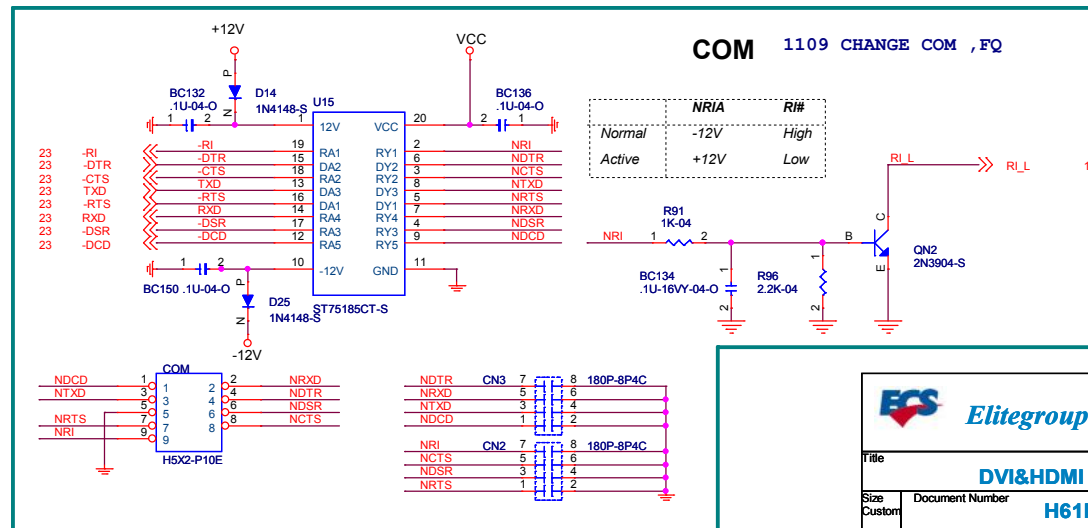
DVI



HDMI

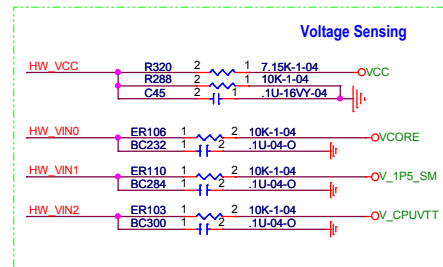
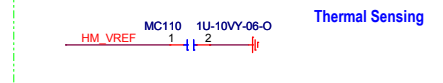
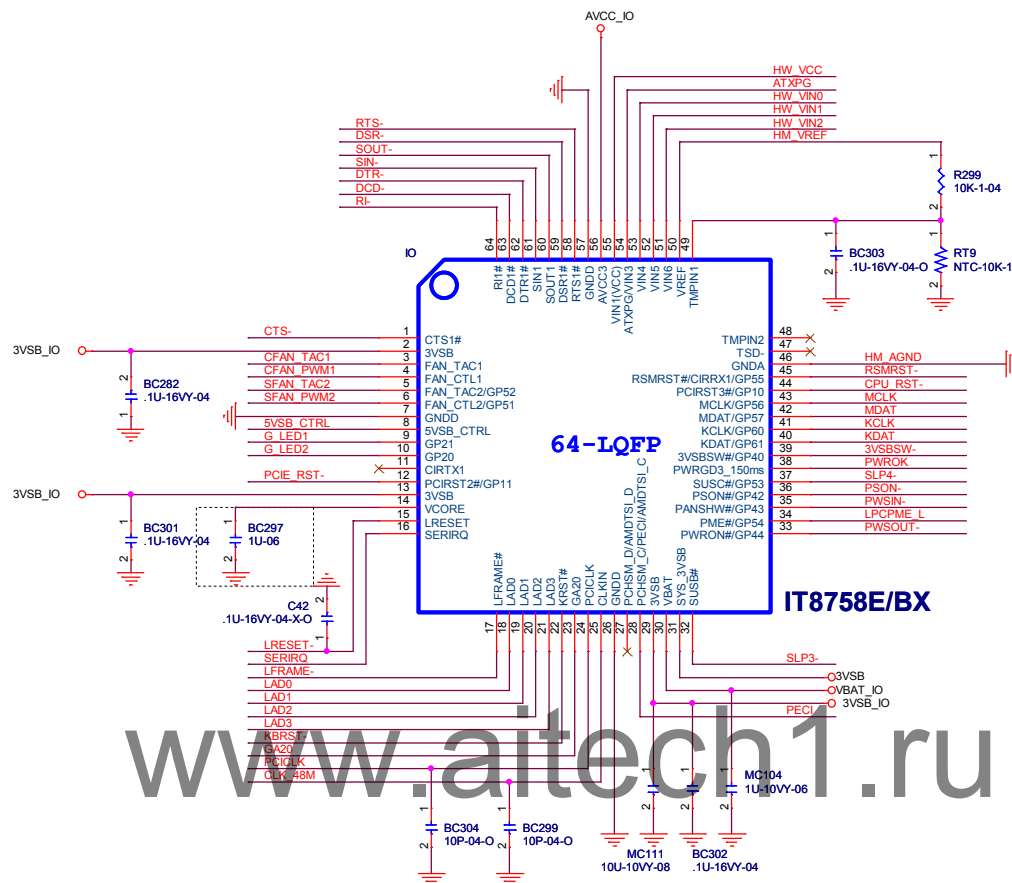
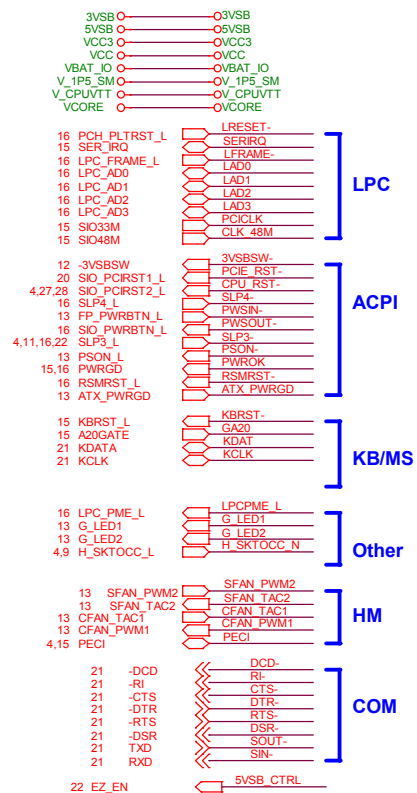


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External Connection

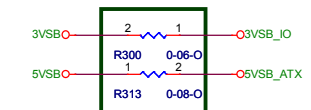


EUP

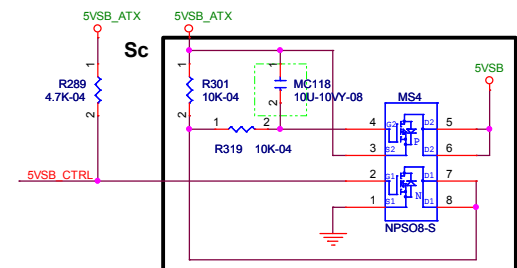
	W/O EUP	W EUP
Sb	V	X
Sc	X	V
Sd	X	V

page 12

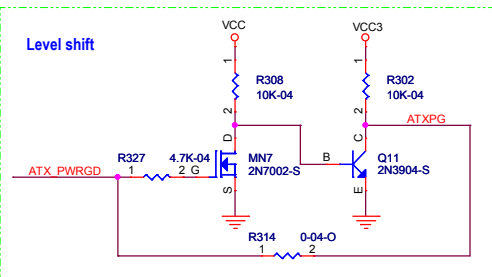
Sb



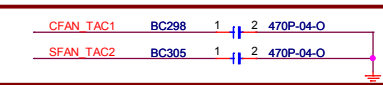
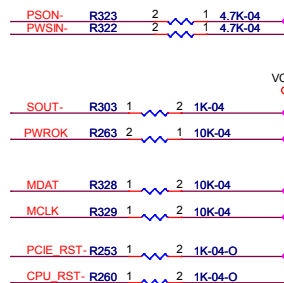
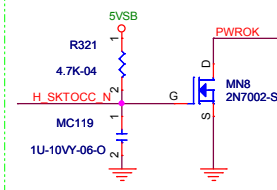
Sc



Level shift



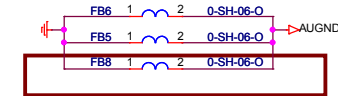
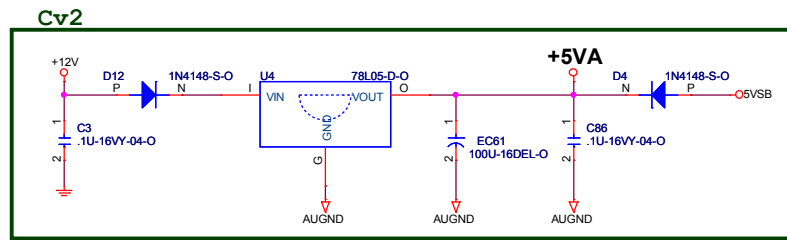
Electric Test







Elitegroup Computer Systems



Title	SIO-IT8758E		
Size	Document Number	H61H2-D	Rev VA
Custom			
Date:	Tuesday, March 01, 2011	Sheet	23 of 31




Pin	Signal	Connection
16	HDA_RST_L	AZ_RST-
16	HDA_BITCLK	AZ_BIT_CLK
16	HDA_SYNC	AZ_SYNC
16	HDA_SDINO	AZ_SDAIN
16	HDA_SDOUT	AZ_SDOUT






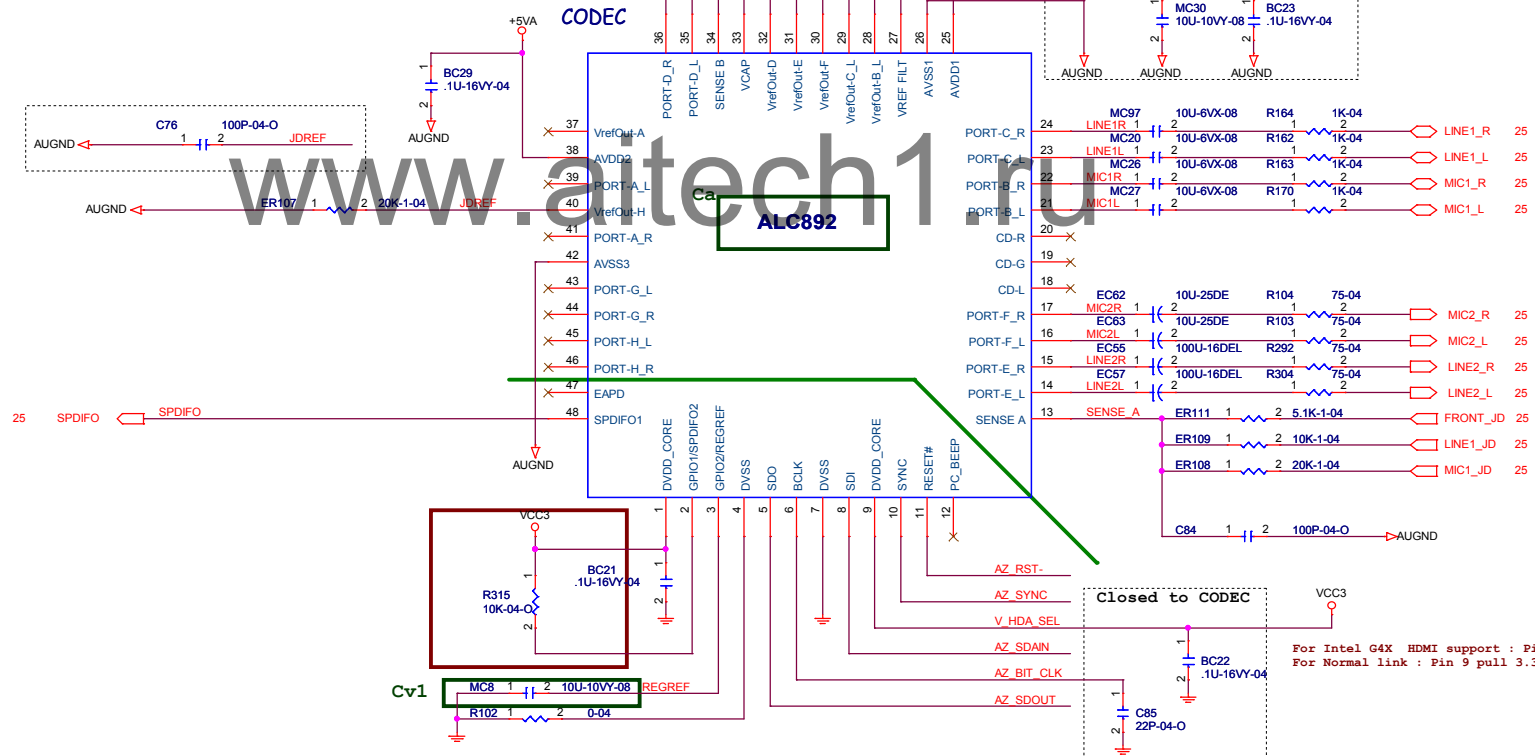
PORT-F 25 MIC2_JD  ER105 1  2 20K-1-04 10U-10V-08-0

PORT-E 25 LINE2_JD  ER104 1  2 39.2K-1-04

AUGND  C83 1  2 100P-04-0 SENSE_B

25 FRONT_L  R291 1  2 75-04 EC51 1  2 10U-25DE FRONTL

25 FRONT_R  R280 1  2 75-04 EC52 1  2 10U-25DE FRONTR



Location	ALC892	ALC662
Ca	ALC892	ALC662
Cb	2.2K-04	3.3K-04
Cv1	V	X
Cv2	X	V
Cv3	V	X

Cb

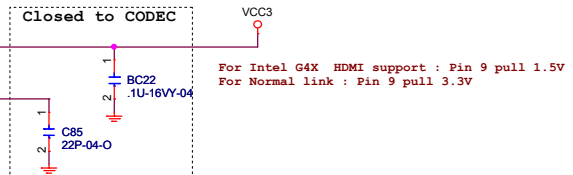
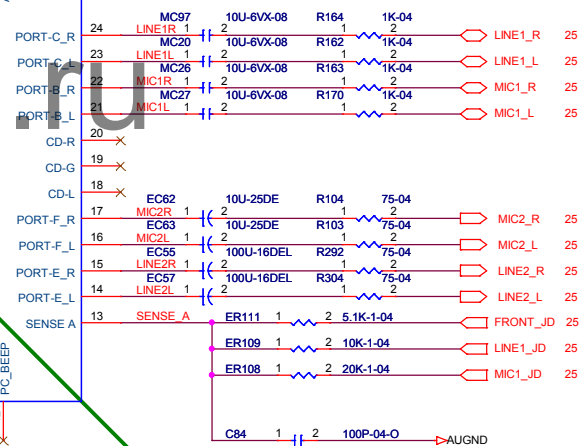
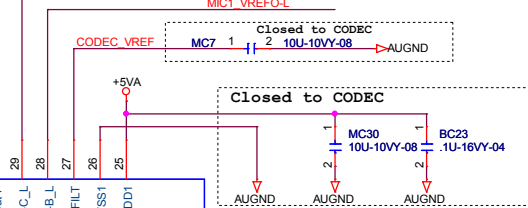
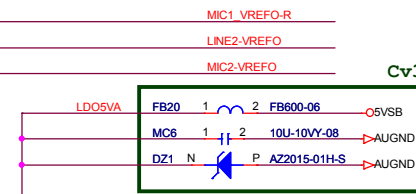
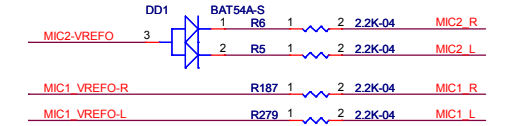
DD2

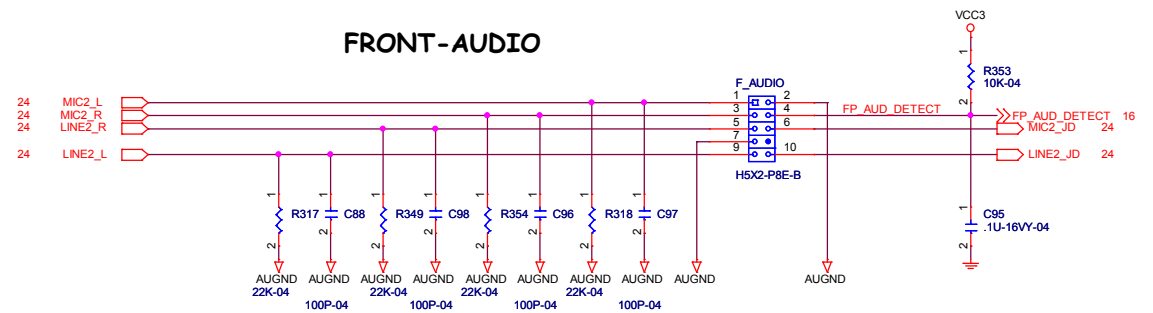
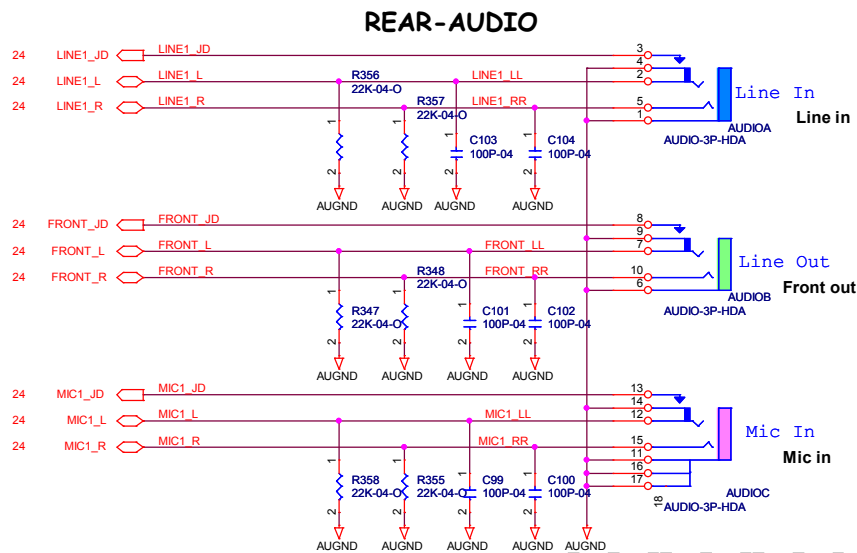
BAT54A-S

1 R12 1 2 2.2K-04 LINE2_R

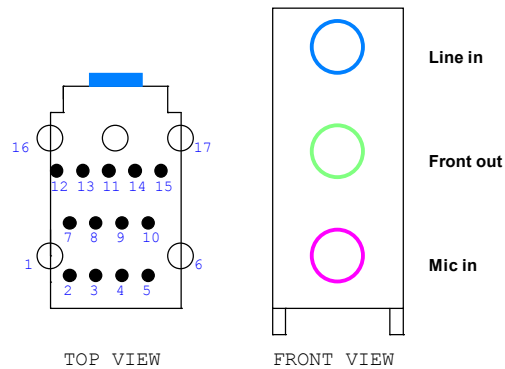
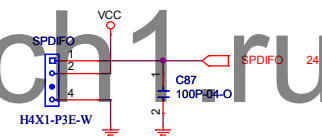
2 R7 1 2 2.2K-04 LINE2_L

LINE2-VREFO 3





SPDIF-OUT



TPM HEADER

Del TPM
By Mao 2011/02/14

LPT HEADER

Del LPT
By Mao 2011/02/22

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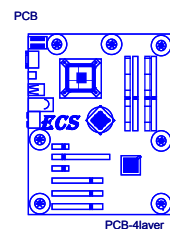
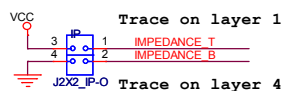
1)Circuit type 1

Layer 1:TOP

Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM



PCB STACK:

L1:TOP

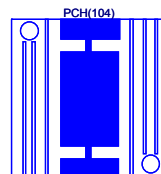
L2:PWR

L3:GND

L4:BOTTOM



JP-WI-P6.25



20-120-011476

5series PN:20-120-010851

CLR_CMOS(1-2)

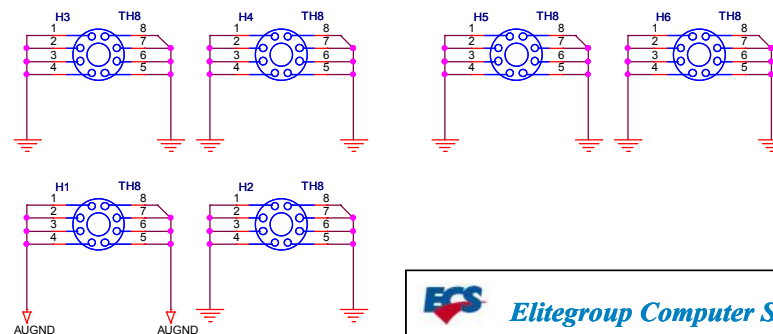


JP-R

BT(104)



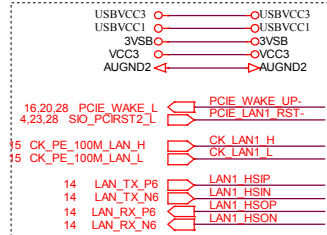
CR2032



Elitegroup Computer Systems

Title		
TPM&LPT&LPC DEBUG &GND&104		
Size	Document Number	Rev
Custom	H61H2-D	V:A
Date:	Tuesday, March 01, 2011	Sheet 26 of 31

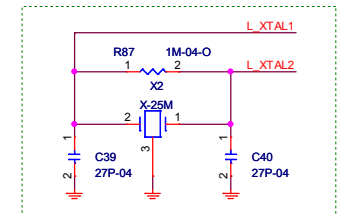
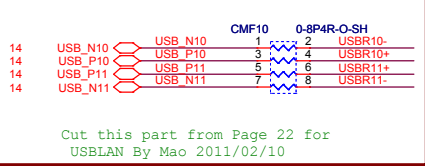
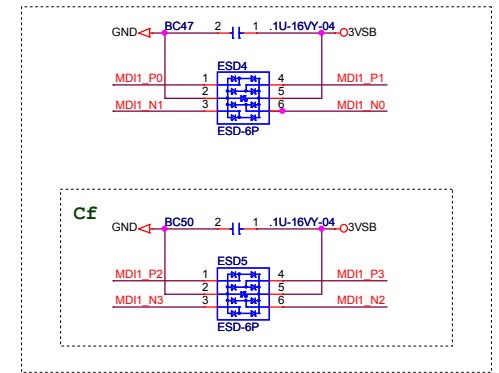
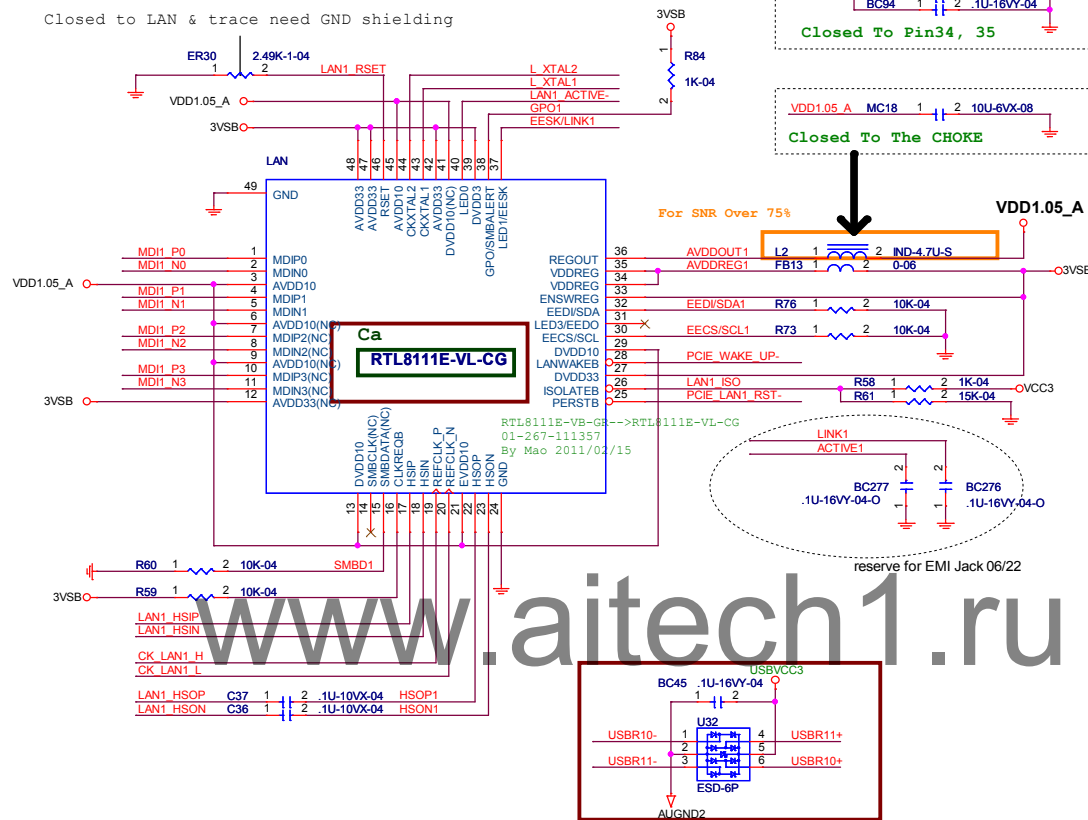
External Connection



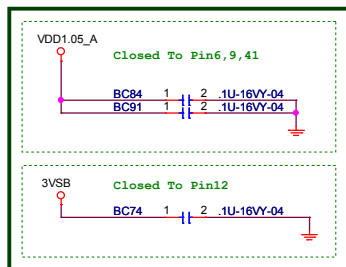
糧も蠹匪:

LAN_HSOP/N叫鎖 SB PCIE RX狼
LAN_HSIP/N叫鎖 SB PCIE TX狼
LAN_HSIP/N SB PCIE TX狼璣癩 AC coupling cap

Closed to LAN & trace need GND shielding

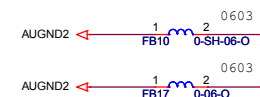
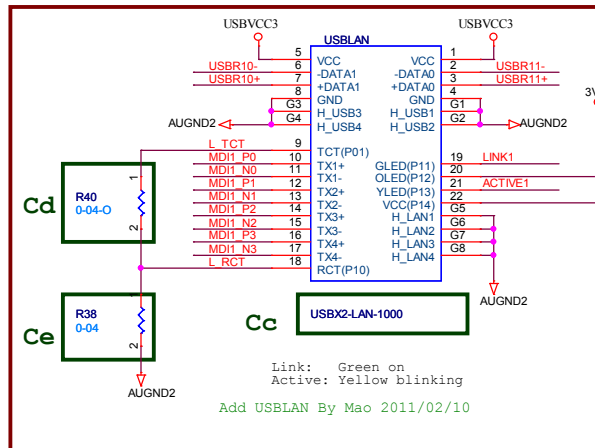
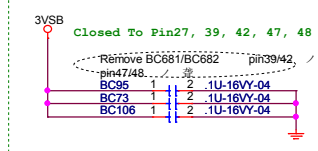
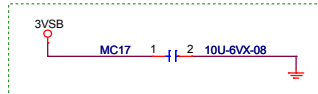
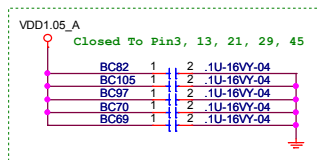


Cb



BOM Difference

	RTL8111E-VL-CG 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-VB-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cf	V	X
Cg		



15 CK_PE_USB3_H >> PCIE_CLK1_P
15 CK_PE_USB3_L >> PCIE_CLK1_N
14 USB3_TX_P3 >> PE1X_TP2
14 USB3_TX_N3 >> PE1X_TN2
14 USB3_RX_P3 >> PE1X_RP2
14 USB3_RX_N3 >> PE1X_RN2
4,23,27 SIO_PCRST2_L >> PCIRST3_L
16,20,27 PCIE_WAKE_L >> PCIE_WAKE_L

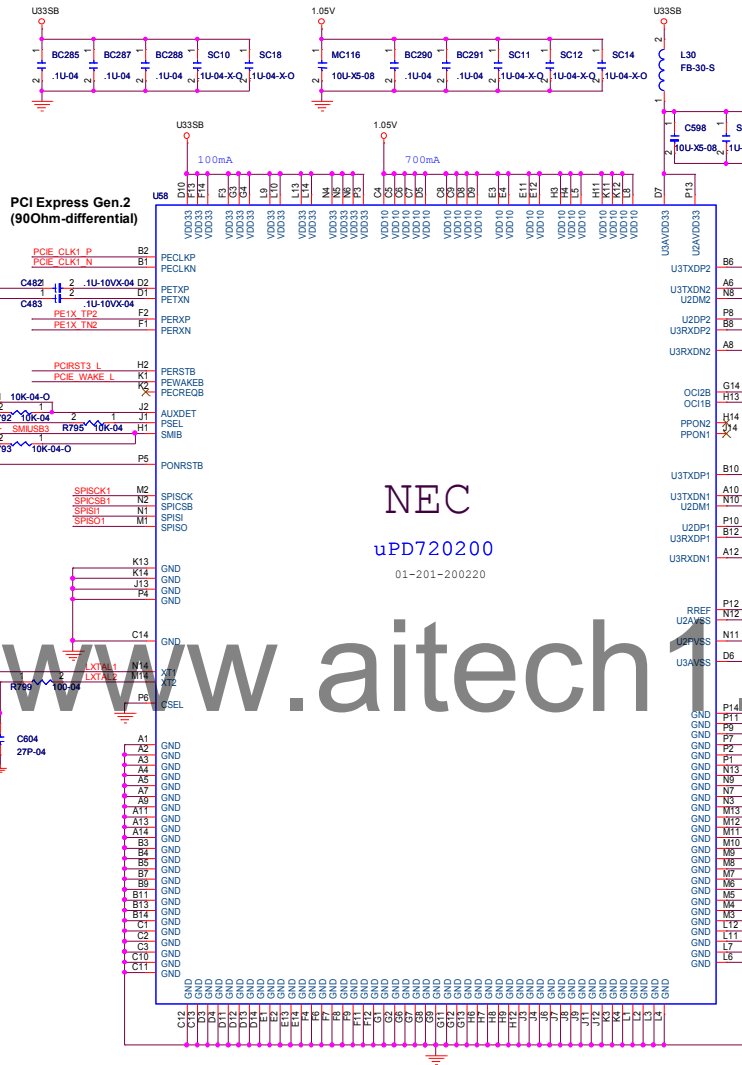
For USB3.0 use

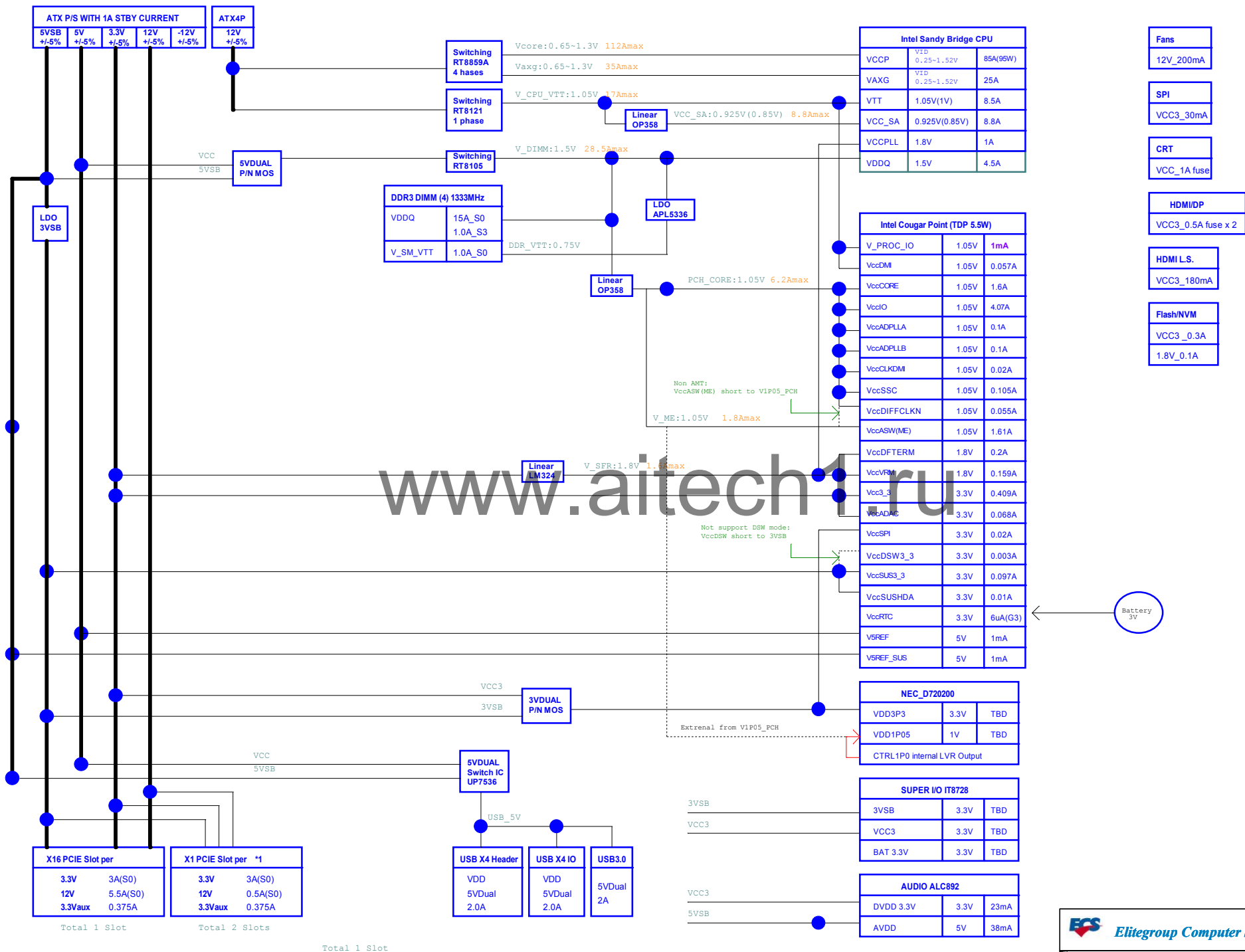
LSRX0+ UI_RP0
LSRX0- UI_RN0
LSRX1+ UI_RP1
LSRX1- UI_RN1
LSTX0+ UI_TP0
LSTX0- UI_TN0
LSTX1+ UI_TP1
LSTX1- UI_TN1

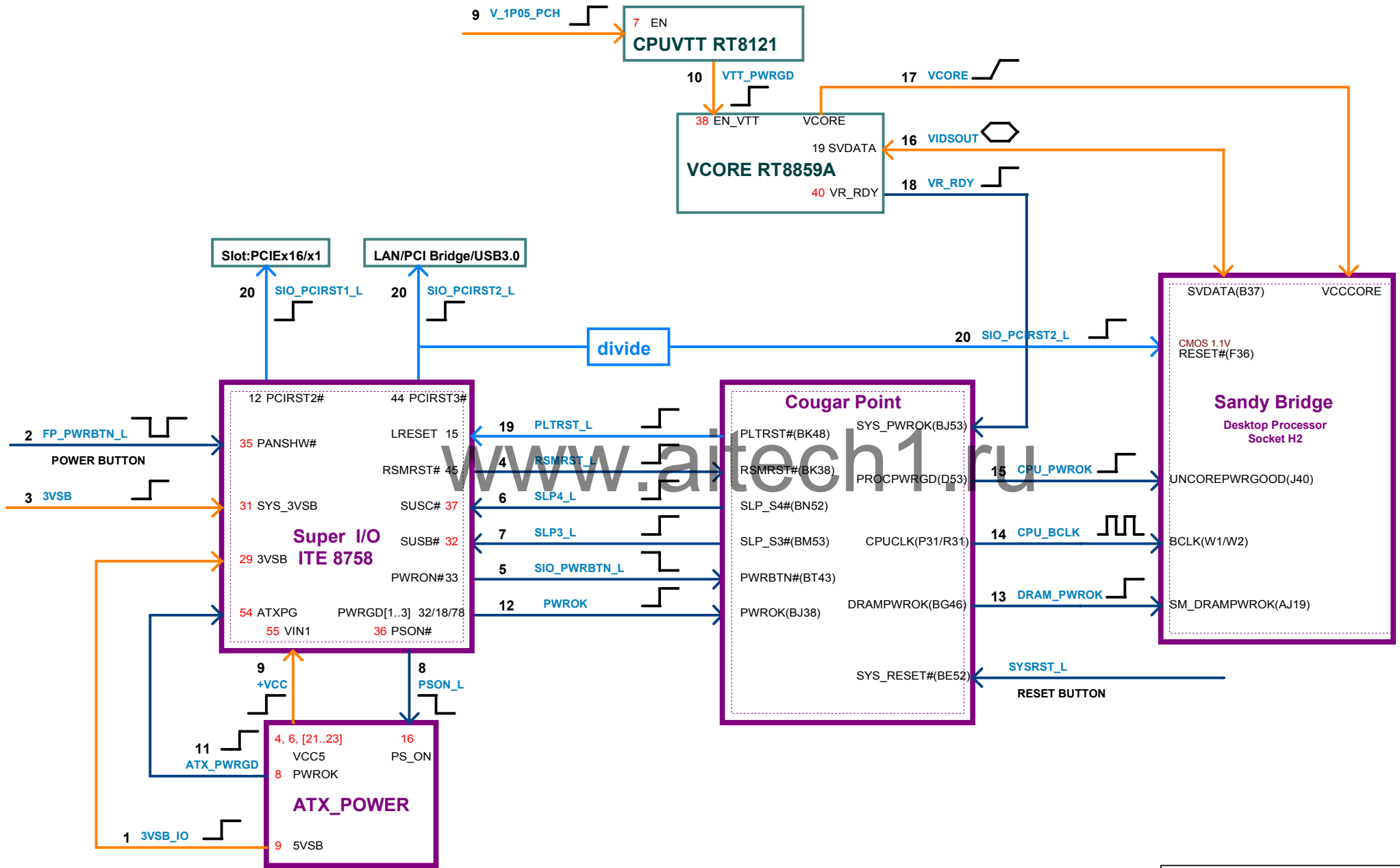
Note:

1. Every Power trace (3.3V, 1.05V, A3.3V, 12V, 5V, VCCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express), should be wired as shortly as possible.
4. Capacitors C100-113 should be located next to U1, and connected to GND tightly -- by tracing shortly and broadly.
5. For signal traces, routing priority is as follows;
USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
> Remove any impairment or discontinuity.
> Keep same length by each other.
> Keep same width and spacing.

For more information please refer to 'USB3.0 Board Design Guide' in design kit.







NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

